

# Facile fabrication of lateral nanowire wrap-gate devices with improved performance

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We present a simple fabrication technique for lateral nanowire wrap-gate devices with high capacitive coupling and field-effect mobility. Our process uses e-beam lithography with a single resist-spinning step, and does not require chemical etching. We measure, in the temperature range 1.5-250 K, a subthreshold slope of 5-54 mV/decade and mobility of 2800-2500  $\text{cm}^2/\text{Vs}$  – significantly larger than previously reported lateral wrap-gate devices. At depletion, the barrier height due to the gated region is proportional to applied wrap-gate voltage.

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Nanowire field effect transistors (NWFETs) have shown promise for device applications in the field of nanoprocessor and sensors<sup>1-4</sup>. Several strategies for improving NWFET device performance have been reported<sup>5-7</sup>. A major challenge is to increase the capacitive coupling between the gate and the nanowire (NW) for a better control of the gate response for high frequency applications<sup>8</sup>. A wrap-gate NWFET, that has a coaxial gate electrode around the NW device, is an ideal device geometry where the gate electrode can control the charge transport effectively. Previous reports on vertical wrap-around gate NWFET devices made on nanowire arrays have shown improved performance. However, the fabrication typically involves several lithography steps<sup>5,6</sup>. In a recent work, Storm *et al.*<sup>9</sup> have successfully fabricated a lateral wrap-gate; such devices demonstrate the potential of wrap-gate NWFET, however; the fabrication process involves several steps of chemical-etching following deposition of oxides and metal onto the as-grown NWs (possible only for NWs which are vertically grown and of low density). It is desirable to develop a generalized method of fabrication that eliminates wet etching and multiple lithographic steps to avoid damage to the surface of the NWs which can result in poor mobility.

In this letter, we report a simple fabrication process for lateral wrap-gate NWFET devices with a single step of resist spinning together with e-beam lithography to define source, drain and gate electrodes without any etching steps. We demonstrate n-type FET behavior with the application of wrap-gate voltage ( $V_g$ ) with a large current on-off ratio ( $5 \times 10^3$ ). In the depletion region, we show how the activation energy, which is a measure of the potential barrier in the gated region with respect to the un-gated parts of the nanowire, varies with the application of  $V_g$ . We characterize the capacitance of

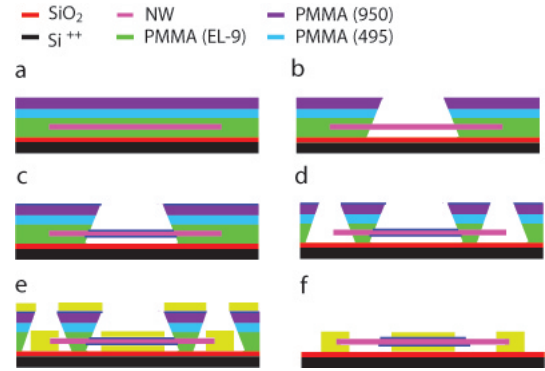


FIG. 1. Various steps of lithography used for fabricating wrap-gate devices. a) Sandwiched nanowire between polymer e-beam resists of different molecular weights. b) The gate electrode is patterned by e-beam and developed using a standard developer. c) 10 nm thick  $\text{HfO}_2$  is conformally coated by ALD. d) The source and drain electrodes are written and developed leading to the structure where the NW is suspended in three segments. e) The deposition of the electrodes using chromium and gold by DC magnetron sputtering leads to fabrication of drain, source and gate electrodes. f) The last step consists of liftoff in acetone to remove the polymer resist and metal layers.

these wrap-gate NWFETs, as well as its subthreshold slope (SS). The temperature variation (1.5-250K) of SS (5-54mV/decade) shows how the performance of these devices improve at low temperatures. The estimated mobility (2800-2500  $\text{cm}^2/\text{Vs}$  over the aforementioned temperature range) is an order of magnitude higher than the recently reported mobility of a wrap-gate device<sup>9</sup>.

InAs nanowires,  $\sim 10 - 15 \mu\text{m}$  long and  $\sim 70-100\text{nm}$  in diameter, are grown via the vapour-liquid-solid technique as described previously<sup>10</sup>. As-grown nanowires are sonicated in isopropanol (IPA) and dispersed on a predefined marker patterned on a 300 nm  $\text{SiO}_2$  substrate coated with PMMA (Microchem EL9). These NWs are then sequentially covered with another 3 layers of PMMA (EL-9,

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PMMA495, PMMA950). Fig. 1a shows the schematic of NW sandwiched between layers of e-beam resist. First, an e-beam exposure is done to define the wrap-gate electrode; this stage allows the length of the wrap-gate, along the length of the NW, to be precisely defined. After developing this exposure in a mixture of methyl isobutyl ketone (MIBK) and IPA, the NW is suspended in the developed region that defines the length of the wrap-gate – as shown in Fig. 1b. A gate dielectric consisting of  $\sim 10$  nm of  $\text{HfO}_2$  is coated conformally around the nanowire by atomic layer deposition (ALD) at a temperature of  $120^\circ\text{C}$  (Fig. 1c). It is critical to use a low-temperature process for  $\text{HfO}_2$  deposition to prevent hard-baking the e-beam resist layers (ALD process is given in supplementary material<sup>11</sup>). Following this, we pattern the source and drain electrodes by another e-beam exposure, through the thin  $\text{HfO}_2$  layer coated all over the resist. The electron beam at 20 kV can expose the underlying polymer resist layers and this is the key reason that our process reduces several steps of fabrication. Another step of e-beam development in MIBK:IPA leads to the formation of patterns for the source and drain electrodes (shown in Fig. 1d). Before depositing the electrodes we use a  $\text{NH}_4\text{S}_x$  treatment for getting better Ohmic contacts (described elsewhere<sup>12</sup>) at the source and drain electrodes and find that this does not compromise the gate dielectric. Deposition of 100 nm Cr and 300 nm Au in a DC sputtering system defines the source, drain and gate electrodes in a single metallization step (a schematic at the end of this step is shown in Fig. 1e). Sputter deposition of metal is critical as the metal clusters have broader momentum distribution and this ensures that the metal is deposited under the NWs leading to a conformal deposition of metal all around the NW at the electrodes. The final step consists of a lift-off in acetone to get the wrap-around gate device (schematic of the device shown in Fig. 1f). The liftoff step crucially depends on the stack of multilayered resist used in sandwiching the NW as described earlier. Fig. 2a shows a scanning electron microscope image of a finished wrap-gate NWFET, also shows the suspended segments between the wrap-gate and other two electrodes (device images with different wrap-gate lengths are shown in supplementary material<sup>11</sup>). The yield of our technique for wrap-gate device is 100 percent. This technique does not require chemical etching and thus applicable not only for InAs but can be used for NWs of other materials as well. Fig. 2a shows a tilted angle SEM of a NWFET and the schematic of the device together with the circuit used for measurement (Fig. 2b). The room temperature response of the source-drain current ( $I_{SD}$ ) with  $V_g$  for different applied source-drain voltage ( $V_{SD}$ ) is shown in Fig. 2c, and demonstrates low voltage operation of a typical NWFET. The I-V shown in Fig. 2d, shows good saturation characteristics, the current on-off ratio being  $\sim 5 \times 10^3$ . We have studied the temperature dependence of the conductance as a function of  $V_g$  down to 1.5K. Fig. 3a shows conductance as a function of  $V_g$ . The temperature vari-

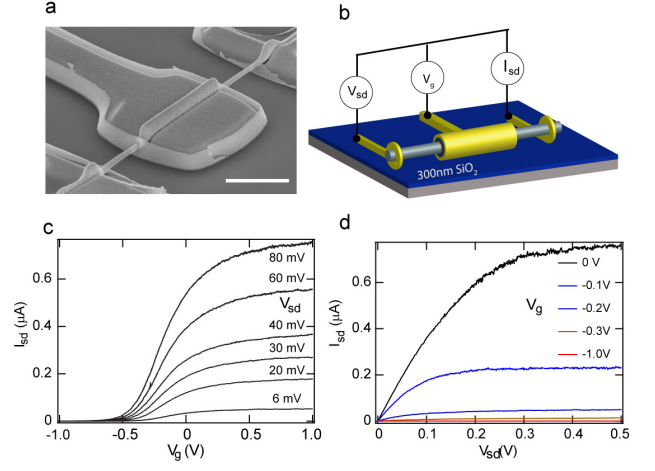


FIG. 2. (a) A tilted SEM image of a device. The scale bar corresponds to  $1 \mu\text{m}$ . The NW is suspended 200 nm above the  $\text{SiO}_2$  substrate. (b) Schematic of the wrap-gate nanowire device and the circuit used for electrical transport. (c) At room temperature,  $I_{SD}$  as a function of  $V_g$  at different applied  $V_{SD}$ . (d) Room temperature I-V characteristic at different applied  $V_g$ , shows good saturation characteristics.

ation of SS (at zero  $V_{SD}$ ) can be seen in the inset of Fig. 3a – a value of 54mV/decade at 250K reduces to 5mV/decade at 1.5K. The conductance is thermally activated near the off state of the FET (see Fig. 3b) due to the potential barrier formed under the wrap-gate (see Fig. 3c). The activation energy decreases linearly with applied  $V_g$  (Fig. 3c); maximum value of  $\sim 0.17$  eV occurs when the device is completely turned off. This shows that the gate can effectively push the Fermi level near the center of the band gap (0.35 eV). The wrap-gate covers the middle part of the NW ( $\sim 4 \mu\text{m}$ ) and this length can be varied in the lithography step (Fig. 1b). By varying the wrap-gate potential, we are changing the conductance  $G_2$  of the active region while the two neighboring segments of the nanowire having conductance  $G_1$  and  $G_3$  are independent of  $V_g$ . This activation behavior can be understood from the schematic of the band diagram of the wrap-gated NW given in the inset of Fig. 3c, together with the resistor model, that is used later to extract field effect mobility. One important parameter of a FET is its capacitive coupling with the gate electrode. We have done a capacitance-voltage (C-V) measurement at room temperature to get an accurate value of capacitance of the dielectric between the wrap-gate electrode and the nanowire. The measured capacitance per unit length is around  $\sim 1.5 \text{ fF}/\mu\text{m}$  (details of the measurement and frequency response is given in supplementary material<sup>11</sup>), much higher than the  $\sim 100 \text{ aF}/\mu\text{m}$  range typically seen in cylinder-on-plane device configurations<sup>13</sup>.

Another parameter to benchmark a FET is its field effect mobility. We have estimated field effect mobility ( $\mu$ ) from the slope of conductance ( $G$ ) vs  $V_g$  plot ( $\frac{dG}{dV_g}$ ), using

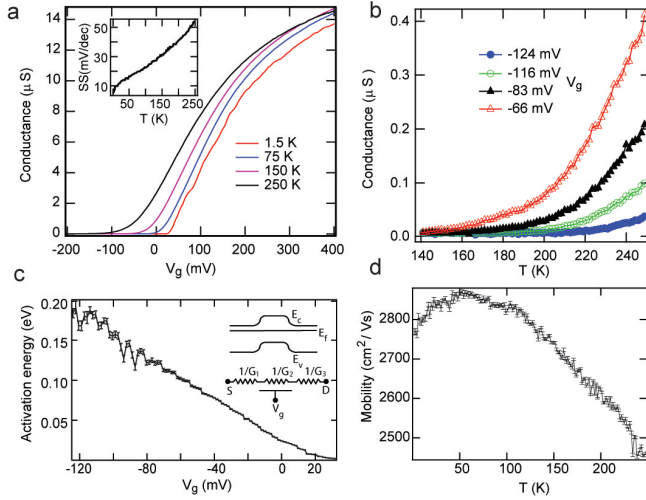


FIG. 3. (a) Field effect transistor (FET) behavior of the device at different temperatures. Inset shows the plot of the subthreshold slope vs temperature. (b) Conductance as a function of temperature when the nanowire is depleted. (c) Shows the variation of the height of the potential barrier as a function of  $V_g$ . Inset shows the cartoon of the band diagram of the device. (d) Plot of field effect mobility as a function of temperature, shows that mobility peaks around 50K.

the expression  $\mu = \frac{L^2}{C} \frac{dG}{dV_g}$ , where  $L$  and  $C$  are the length of the nanowire and capacitance of the gate dielectric respectively. The  $\frac{dG}{dV_g}$ , only due to the active part of the NWFET, is estimated assuming that at some  $V_g$  near flat band, the wire will conduct homogeneously in all the three parts (this assumption gives us only a lower bound to the mobility; details are given in supplementary material<sup>11</sup>).

Fig. 3d shows the field effect mobility value 2500-2800  $\text{cm}^2/\text{Vs}$ , this is comparable to the value obtained previously on standard InAs NWFET of cylinder-on-plane geometry<sup>10,14</sup>. The mobility of our devices is an order of magnitude larger than the recently reported mobility ( $\sim 109 \text{ cm}^2/\text{Vs}$ ) of a wrap-gated device<sup>9</sup>, where the fabrication process involved many wet etching steps which can potentially introduce more surface states and thus enhance surface scattering. However it is less than the highest mobility value reported so far<sup>13,15</sup> on InAs nanowires. It is known that the reason for reduction of mobility in InAs nanowire from its bulk value is that the surface accumulation charge contributes significantly in electrical conduction, and due to the scattering at the surface the mobility reduces. As a result mobility increases with the wire diameter<sup>13</sup>. A possible reason for the lower mobility in our case even with a relatively larger diameter of the nanowire ( $\sim 70 \text{ nm}$ ) is presumably due to the fact that the twin defect density also increases with the diameter, these twin defects result in additional scattering and a reduction in mobility<sup>14,16</sup>. Plot of field effect mobility as a function of temperature, shows that mobility peaks around 50K; a similar trend in the mobility was also observed in a previous work<sup>13</sup>, and it is attributed

to scattering due to surface roughness as well as twin defects.

In conclusion, we have developed a simple fabrication technique for lateral wrap-gate NWFET that can be used for a variety of NW systems. The good capacitive coupling of our devices, and the FET performance including sub-threshold slope and mobility suggest the potential use for high-frequency NWFETs. In addition, such devices with good characteristics at cryogenic temperatures can be used to fabricate on-chip amplifiers for sensitive measurement of current<sup>17</sup> and capacitance<sup>18</sup>. The wrap-gate controlled large electric field will be interesting to study the physics of spin and charge in quasi 1-D systems with spin-orbit interaction<sup>19,20</sup>.

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